

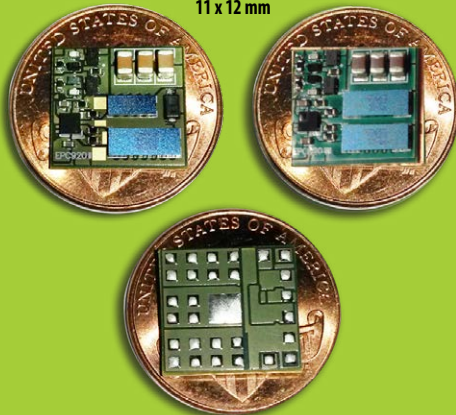
DrGaN^{PLUS} Development Board EPC9201/3 Quick Start Guide

Optimized Half-Bridge Circuit for eGaN[®] FETs

EPC9201 Top side

EPC9203 Top side

11 x 12 mm



Mounting side



DESCRIPTION

This development board, measuring 11 x 12 mm, contains two enhancement mode (eGaN®) field effect transistors (FETs) arranged in a half bridge configuration with an onboard Texas Instruments LM5113 gate drive and is driven by a single PWM input. The purpose of these development boards is to simplify the evaluation process by optimizing the layout and including all the critical components on a single board that can be easily connected into any existing converter. A complete block diagram of the circuit is given in figure 1.

For more information on EPC's family of eGaN FETs and ICs, please refer to the datasheets available from EPC at www.epc-co.com. The data-sheet should be read in conjunction with this quick start guide

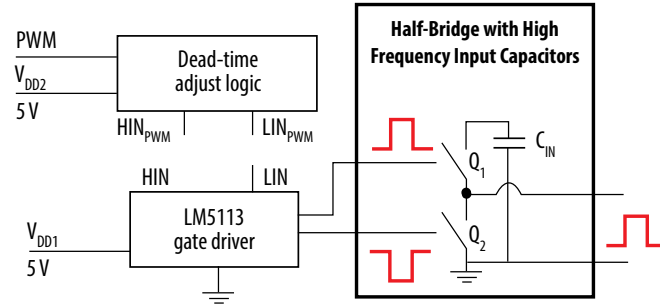


Figure 1: Block diagram of EPC9201/3 development board.

THERMAL CONSIDERATIONS

The development board is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150°C.

NOTE: The development board does not have any current or thermal protection on board.

Table 1: Performance Summary ($T_A = 25^\circ\text{C}$) EPC9201/3

Symbol	Parameter	Conditions	Min	Max	Units
V_{DD}	Gate Drive Input Supply Range		4.5	5	V
V_{INP}	Bus Input Voltage Range	When using 30 V rated EPC9201		20*	V
		When using 80 V rated EPC9203		60*	V
V_{OUT}	Switch Node Output Voltage	When using 30 V rated EPC9201		30	V
		When using 80 V rated EPC9203		80	V
I_{OUT}	Switch Node Output Current	When using 30 V rated EPC9201		40*	A
		When using 80 V rated EPC9203		20*	A
V_{PWM}	PWM Logic Input Voltage Threshold	Input 'High'	3.5	6	V
		Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	VPWM rise and fall time < 10 ns	60		ns
	Minimum 'Low' State Input Pulse Width	VPWM rise and fall time < 10 ns	200#		ns

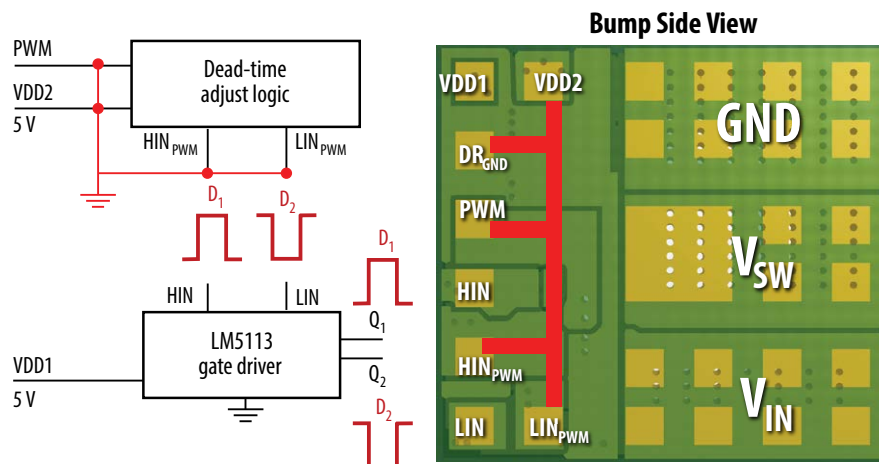
* Assumes inductive load, maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermal.

Limited by time needed to 'refresh' high side bootstrap supply voltage.

Bump Side View

The schematic diagram illustrates the electrical connections for the gate driver. A PWM input signal (D) is connected to the Dead-time adjust logic block and the LM5113 gate driver. The logic block also receives VDD2 and 5V, and outputs HIN_PWM and LIN_PWM to the gate driver. The gate driver also receives VDD1 and 5V, and outputs Q1 and Q2. The bump side view shows the physical layout with labels for VDD1, VDD2, DR_GND, PWM, HIN, HIN_PWM, LIN, LIN_PWM, and VIN, along with a GND pad and a VSW region.

NOTE: Single PWM timing optimized for most buck converter applications.
For other applications or desired timing settings, two PWM input setting recommended.



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TYPICAL PERFORMANCE

EPC9201

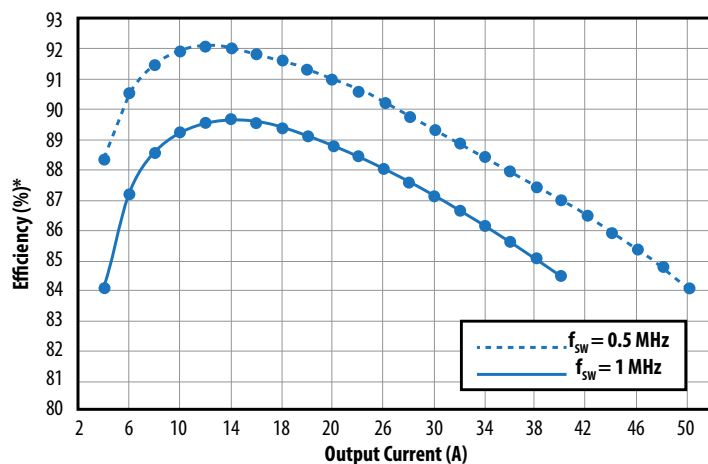


Figure 6: Typical efficiency for $V_{IN} = 12$ V to $V_{OUT} = 1$ V, $L = 250$ nH

*Total system efficiency including power stage, inductor, driver, capacitors, and PCB losses.

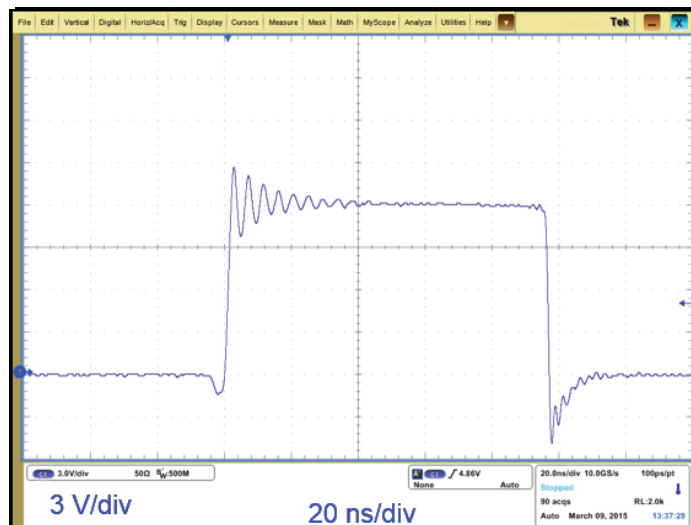


Figure 4: Typical switch node voltage waveform for

$V_{IN} = 12$ V to $V_{OUT} = 1$ V, $I_{OUT} = 40$ A, $f_{SW} = 1$ MHz buck converter.

EPC9203

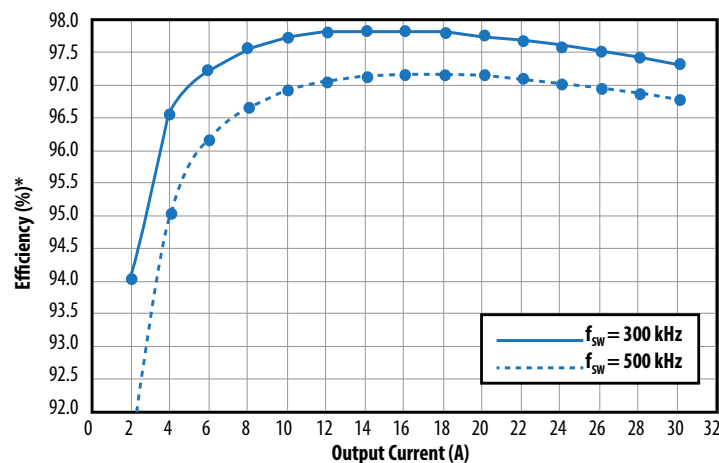


Figure 7: Typical efficiency for $V_{IN} = 48$ V to $V_{OUT} = 12$ V, $L = 4.7$ μ H

*Total system efficiency including power stage, inductor, driver, capacitors, and PCB losses.

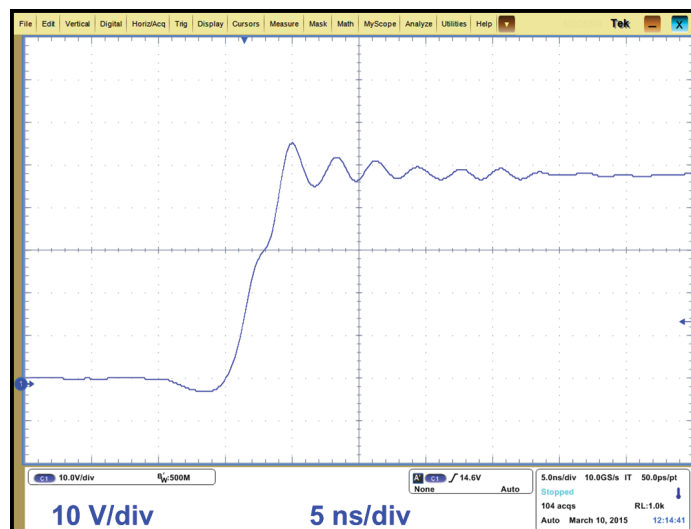


Figure 5: Typical switch node voltage waveform for

$V_{IN} = 48$ V to $V_{OUT} = 12$ V, $I_{OUT} = 20$ A, $f_{SW} = 500$ kHz buck converter

DESIGN CONSIDERATIONS

To improve the electrical and thermal performance of the DrGaN^{PLUS} development board some design considerations are recommended:

1. Large copper planes should be connected to the development board to improve thermal performance as shown in figures 8 through 11. If filled vias are used in the board design, thermal vias should be placed under the device as shown in figure 8 to better distribute heat through buried inner layers. For a design without filled vias, thermal vias should be located outside of the development board.
2. To reduce conduction losses, the inductor and output capacitors should be located in close proximity to the development board.
3. The smaller IC ground connection (pin 6 in mechanical drawings), should be isolated from the power ground connection (pin 3 in mechanical drawings).
4. If additional input filter capacitance is required, it can be placed outside the module. Due to the internal on-board input capacitance, minimizing the distance of the additional input capacitors to the development board, while preferred, is not a design requirement.

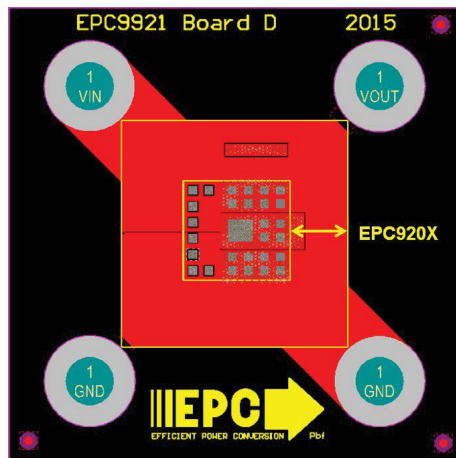


Figure 8: Top layer without filled thermal vias.

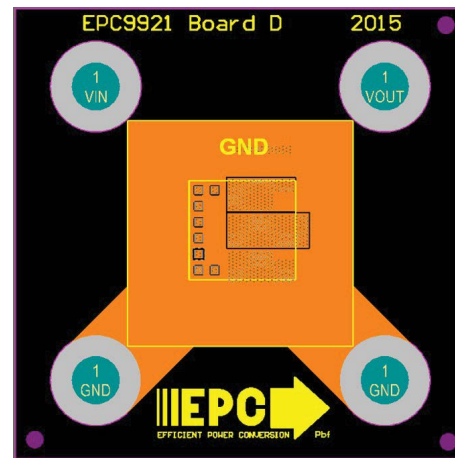


Figure 9: Inner layout 1 layout.

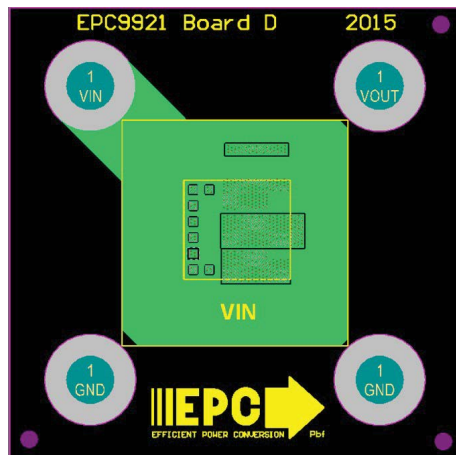


Figure 10: Inner layout 2 layout.

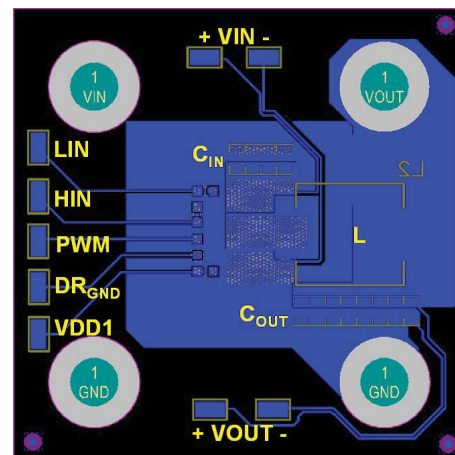
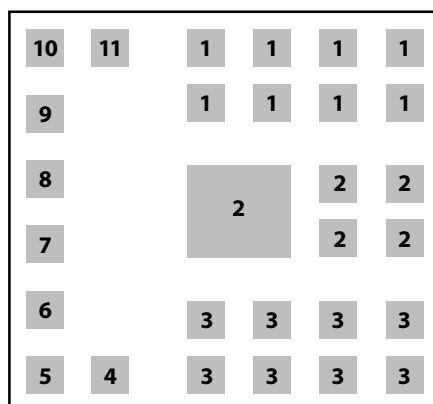
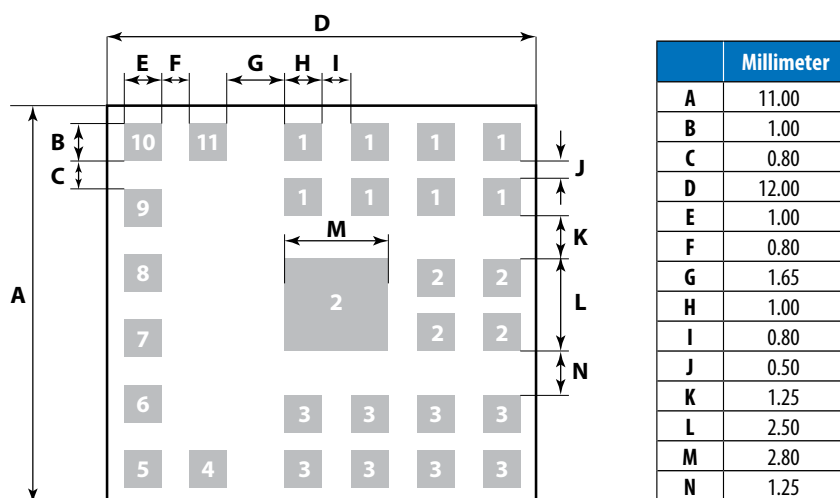


Figure 11: Bottom layer layout.



- Pin 1: Input Voltage, V_{IN}
 Pin 2: Switching Node, V_{SW}
 Pin 3: Power Ground, P_{GND}
 Pin 4: Driver Voltage, V_{DD2}
 Pin 5: Driver Voltage, V_{DD1}
 Pin 6: Driver Ground, DR_{GND}
 Pin 7: PWM Input, PWM
 Pin 8: High Side Input, HIN
 Pin 9: PWM High Side Input, HIN_{PWN}
 Pin 10: Low Side Input, LIN
 Pin 11: PWM Low Side Input, LIN_{PWN}

Table 3: Bill of Materials - EPC9201/3

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	3	CIN1, CIN2, CIN3	Capacitor, 4.7 μ F, 10%, 50 V, X5R, 0805 (EPC9201) Capacitor, 1 μ F, 20%, 100 V, X7S, 0805 (EPC9203)	TDK	C2012X5R1H475K125AB (EPC9201) C2012X7S2A105M125AB (EPC9203)
2	2	Q1, Q2	EPC9201: 40 V 33 A eGaN FET / 30 V 60 A eGaN FET EPC9203: 80 V 60 A eGaN FET	EPC	EPC2015C / EPC2023 (EPC9201) EPC2021 (EPC9203)
3	4	R19, R20, R23, R24	Resistor, 0 Ω , 1/16 W	Stackpole	RMCF0402ZTOR00TR
4	1	C9	Capacitor, 0.1 μ F, 10%, 25 V, X5R	TDK	C1005X5R1E104K050BC
5	1	C19	Capacitor, 1 μ F, 10%, 16 V, X5R	TDK	C1005X5R1C105K050BC
6	1	U2	I.C., Gate driver	Texas Instruments	LM5113
7	2	D1, D2	Diode Schottky 40 V 0.12 A SOD882	NXP	BAS40L,315
8	1	U4	IC GATE AND UHS 2-INP 6-MICROPAK	Fairchild	NC7SZ08L6X
9	1	U1	IC GATE NAND UHS 2-INP 6MICROPAK	Fairchild	NC7SZ00L6X
10	1	R1	Resistor, 10K Ω 1/20 W 1% 0201	Stackpole	MCFO201FT10K0
11	2	C6, C7	Capacitor, CER 100 pF 50 V 5% NP0 0402	Murata	GRM1555C1H101JA01D
12	1	D3	Schottky Diode, 30 V, 2 A MICROSMP (EPC9201 only)	Vishay	MSS2P3-M3/89A
13	1	R4	Resistor, 3.92 Ω 1/16 W 1% 0402 SMD	Stackpole	RMCF0402FT3R92
14	1	R5	Resistor, 20 Ω 1/16 W 1% 0402 SMD (EPC9201) Resistor, 100 Ω 1/16 W 1% 0402 SMD (EPC9203)	Stackpole	RMCF0402FT20R0CT (EPC9201) RMCF0402FT100R0CT (EPC9203)

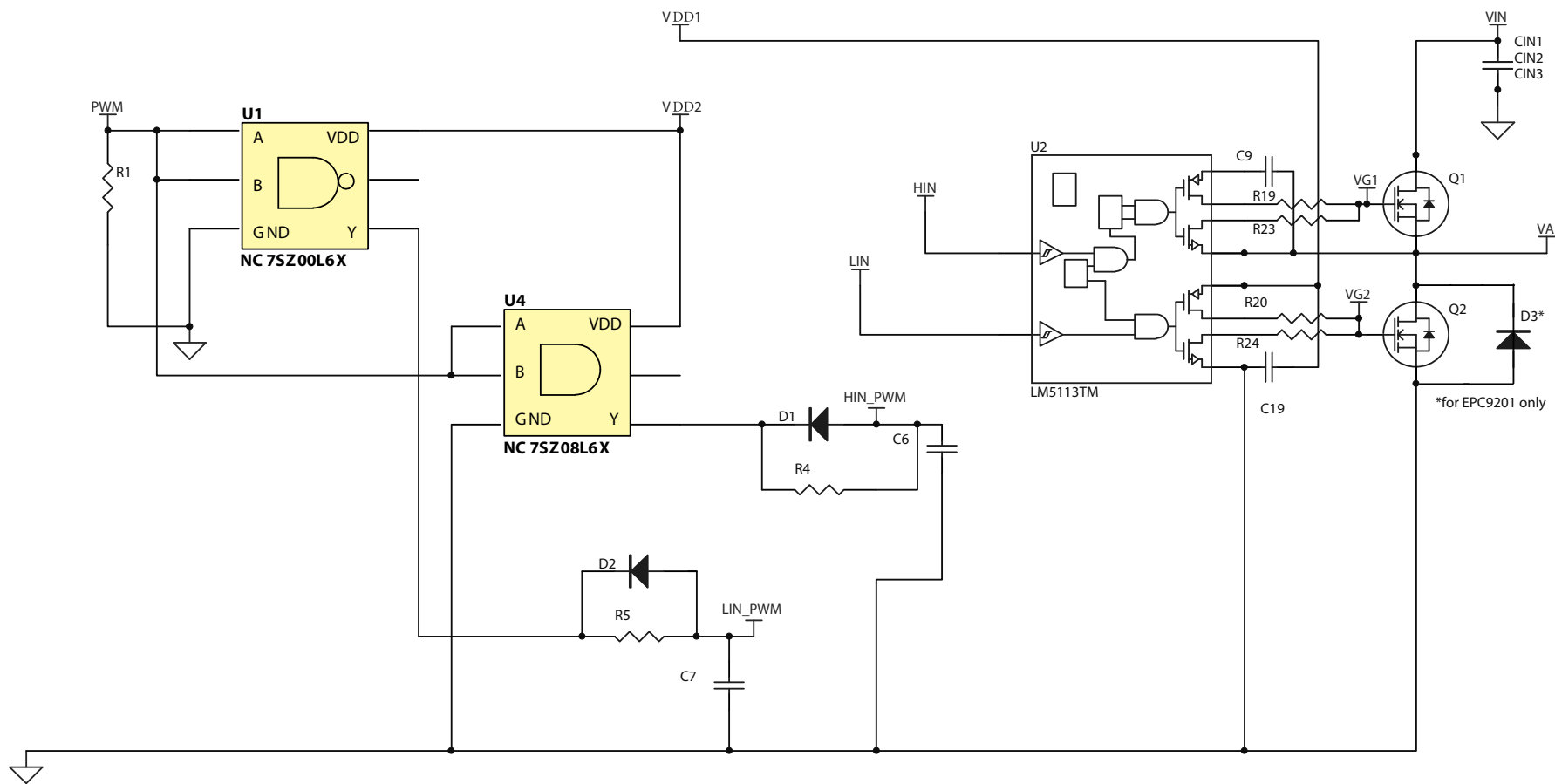


Figure 12: Full schematic EPC9201/EPC9203 Rev 2