

PRODUCT SPECIFICATIONS

For Customer: _____

☐ : APPROVAL FOR SPECIFICATION

Customer Model No. _____

☐ : APPROVAL FOR SAMPLE

 Module No.: ZW-T034TQH-01CP
Date : 2017-07-26

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For Customer's Acceptance:

Approved By	Comment

PREPARED	CHECKED	VERIFIED BY QA DEPT	VERIFIED BY R&D DEPT
John	Techshu		Dmjiaing

2. Revision Record

Date	Rev.No.	Page	Revision Items	Prepared
2017-07-26	V0		The first release	ZHP
DRAFT				

3. General Specifications

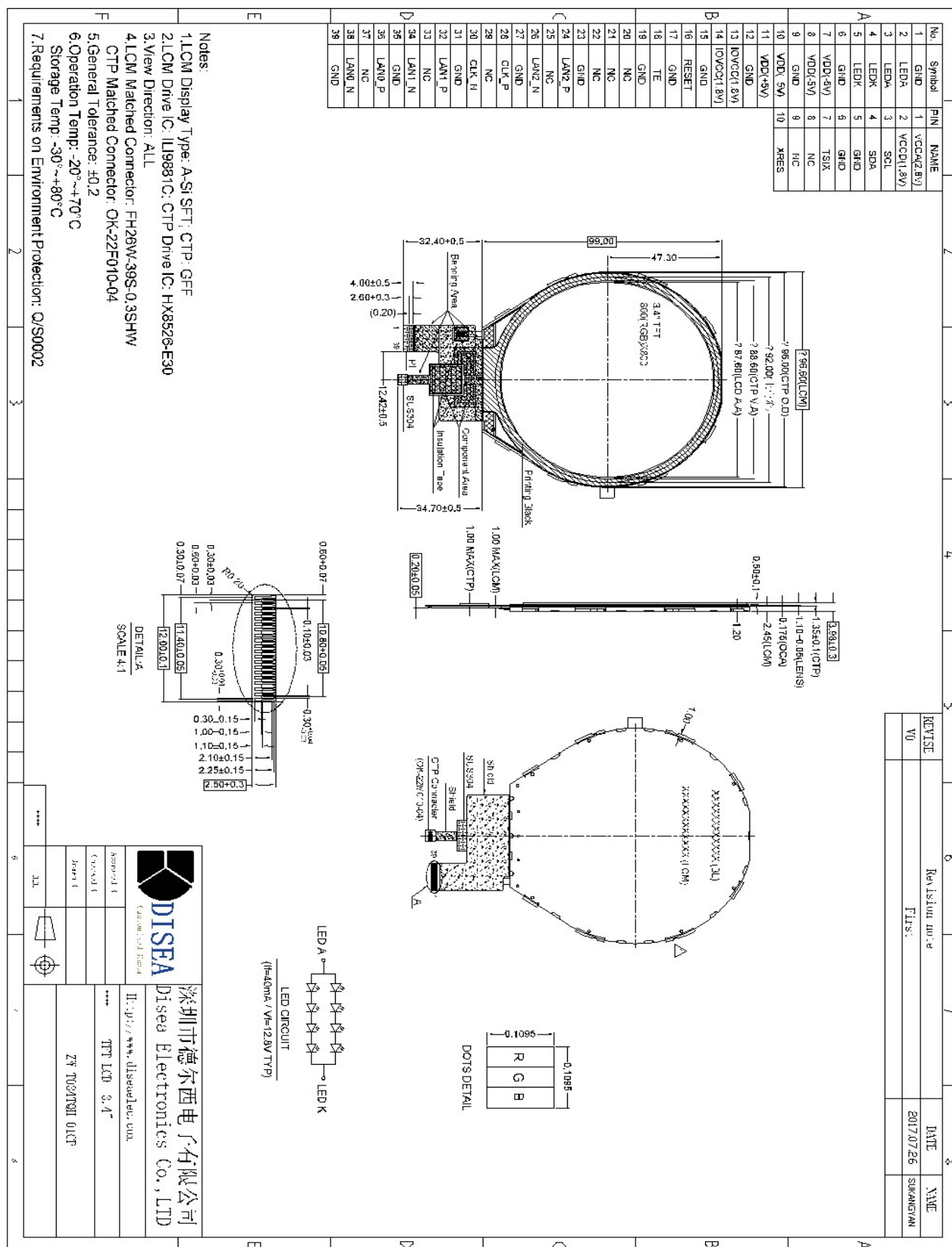
ZW-T034TQH-01CP is a TFT-LCD module. It is composed of a TFT-LCD panel, Touch panel, driver IC, FPC, a back light unit. The 3.4" display area contains 800x 800 pixels and can display up to 16.7M colors. This product accords with RoHS environmental criterion.

Item	Contents	Unit	Note
LCD Type	TFT	-	
Display color	16.7M		
Viewing Direction	FREE	O'Clock	
Operating temperature	-20~+70	°C	
Storage temperature	-30~+80	°C	
Module size	Refer to outline drawing	mm	
Active Area(W×H)	87.6*87.6	mm	
Number of Dots	800(RGB) x 800	dots	
LCM Controller	ILI9881C	-	
C-TP Controller	HX8526-E30		
Power Supply Voltage	3.3	V	
Outline Dimensions	Refer to outline drawing	-	
Backlight	8-LEDs (white)	pcs	
Weight	---	g	
LCM Interface	MIPI-3LINE	-	
C-TP Interface	IIC	-	

Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: Without FPC and Solder.

4.Outline.Drawing



5. Absolute Maximum Ratings($T_a=25^{\circ}\text{C}$)

5.1 Electrical Absolute Maximum Ratings.($V_{ss}=0\text{V}$, $T_a=25^{\circ}\text{C}$)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	-0.3	3.6	V	1, 2
Power Supply Voltage for LCD	V_{op}	-	-	V	

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. $V_{CC} > V_{SS}$ must be maintained.
3. Please be sure users are grounded when handing LCD Module.

5.2 Environmental Absolute Maximum Ratings.

Item	Storage		Operating		Note
	MIN.	MAX.	MIN.	MAX.	
Ambient Temperature	-30°C	80°C	-20°C	70°C	1,2
Humidity	-	-	-	-	3

1. The response time will become lower when operated at low temperature.
2. Background color changes slightly depending on ambient temperature.
The phenomenon is reversible.
3. $T_a \leq 40^{\circ}\text{C}$: 85%RH MAX.
 $T_a \geq 40^{\circ}\text{C}$: Absolute humidity must be lower than the humidity of 85%RH at 40°C .

6. Electrical Specifications and Instruction Code

6.1 Electrical characteristics($V_{SS}=0V$, $T_a=25^{\circ}C$)

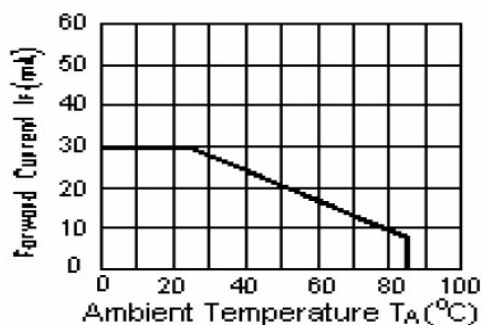
Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Power supply	VDD	$T_a=25^{\circ}C$	3.0	3.3	3.6	V	
Input voltage	'H'	V_{IH}	$V_{DD}=3.3V$	0.7V _{DD}	-	V _{DD}	V
	'L'	V_{IL}	$V_{DD}=3.3V$	0	-	0.3V _{DD}	V
Current Consumption	I _{DD1}	Normal mode	-	--	--	mA	
	I _{DD2}	Sleep mode	-	--	--	mA	
Clock Frequency	f _{CLK}	-	8	9	12	MHz	

Note:

1: Tested in 1×1 chessboard pattern.

6.2 LED backlight specification($V_{SS}=0V$, $T_a=25^{\circ}C$)

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply voltage	V _f	I _f =2X20mA	-	12.8	-	V	
Uniformity	Δ Bp	I _f =2X20mA	80			%	
Luminance for LCD (with TP)	L _v	I _f =2X20mA	-	350		Cd/m ²	
Life Time	time	I _f =2X20mA		20000		hours	1



6.3 Interface signals

Pin No.	Symbol	I/O	Function
1	GND	P	Ground
2~3	LEDA	P	LED Anode
4~5	LEDK	P	LED Cathode
6	GND	P	Ground
7~8	VDD(-5V)	P	-5V INPUT
9	GND	P	Ground
10~11	VDD(+5V)	P	+5V INPUT
12	GND	P	Ground
13~14	IOVCC	P	Power supply 1.8V
15	GND	P	Ground
16	DRESET	I	Global Reset Pin
17	GND	P	Ground
18	TE	I	Global Reset Pin
19	GND	P	Ground
20~22	NC	-	No connection.
23	GND	P	Ground.
24	LAN2_P	I	LAN2_P
25	NC	-	No connection.
26	LAN2_N	I	MIPI lane 2-
27	GND	P	Ground
28	CLK_P	I	MIPI clock +
29	NC	-	No connection.
30	CLK_N	I	IMIPi clock -
31	GND	P	Ground
32	LAN1_P	I	MIPI lane 1+
33	NC	-	No connection.
34	LAN1_N	I	MIPI lane 1-
35	GND	P	Ground
36	LAN0_P	I	MIPI lane 0+
37	NC	-	No connection.
38	LAN0_N	I	MIPI lane 0-
39	GND	P	Ground

CTP Interface

Pin No	Symbol
1	VCCA(2.8V)
2	VCCD(1.8V)
3	SCL
4	SDA
5	GND
6	GND
7	TSIX
8	NC
9	NC
10	XRES

6.4 Timing Chart

6.4.1 MIPI Data to clock Timing Definition

A, High Speed Mode

High Speed Mode – Clock Channel Timing

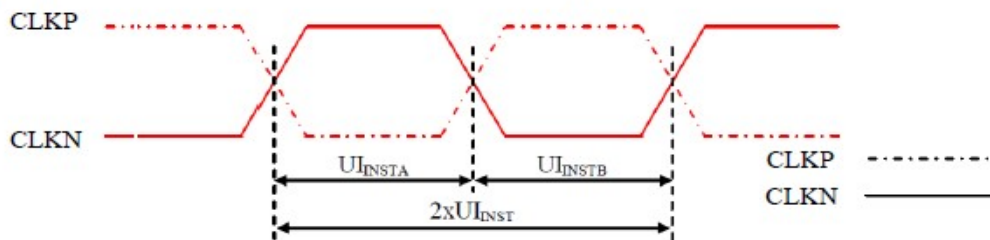


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. $UI = UI_{INSTA} = UI_{INSTB}$
2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

High Speed Mode – Data Clock Channel Timing

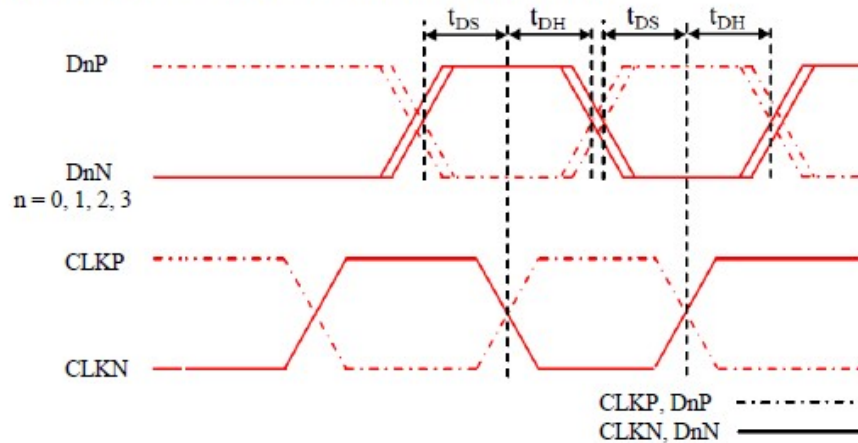


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N, n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rising and Falling Timings

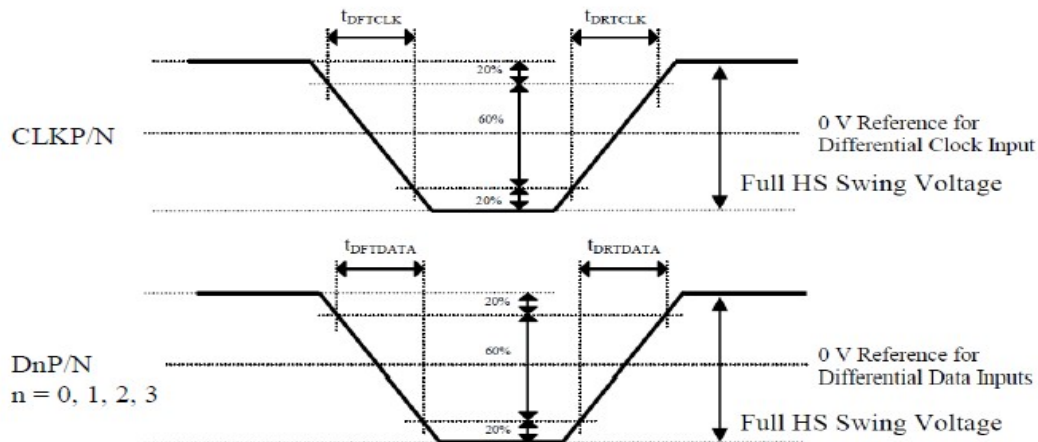


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

6.4.2 Low Speed Mode

Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

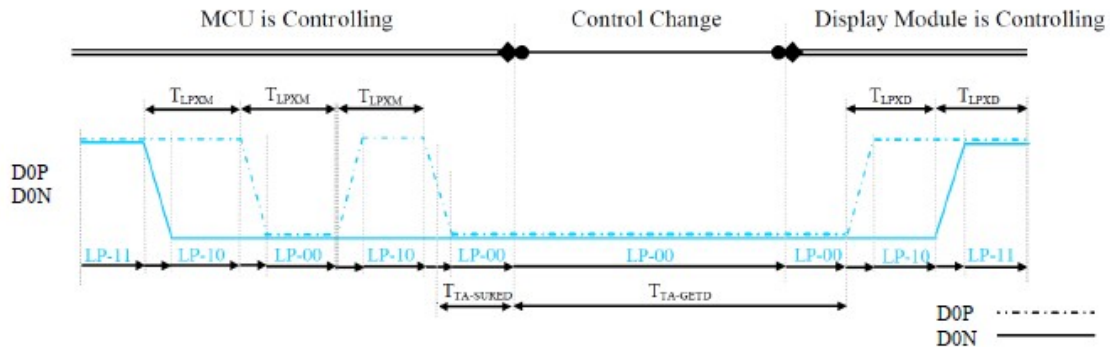


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

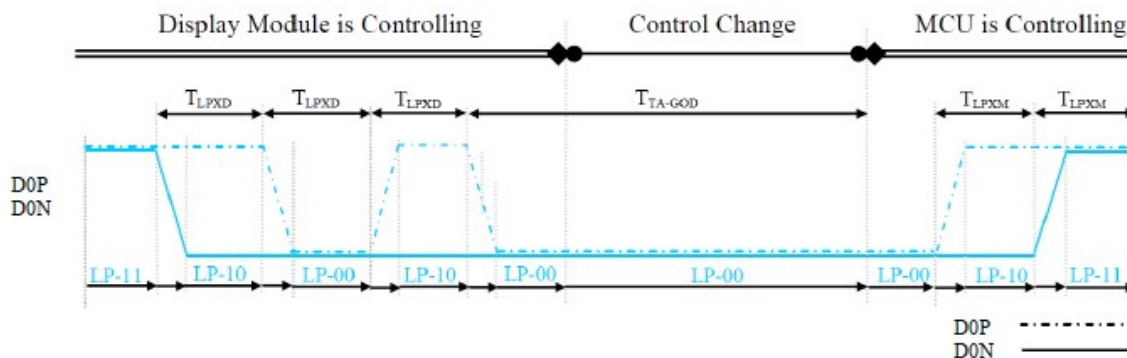


Figure 122: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5 \times T_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

Data Lanes from High Speed Mode to Low Power Mode

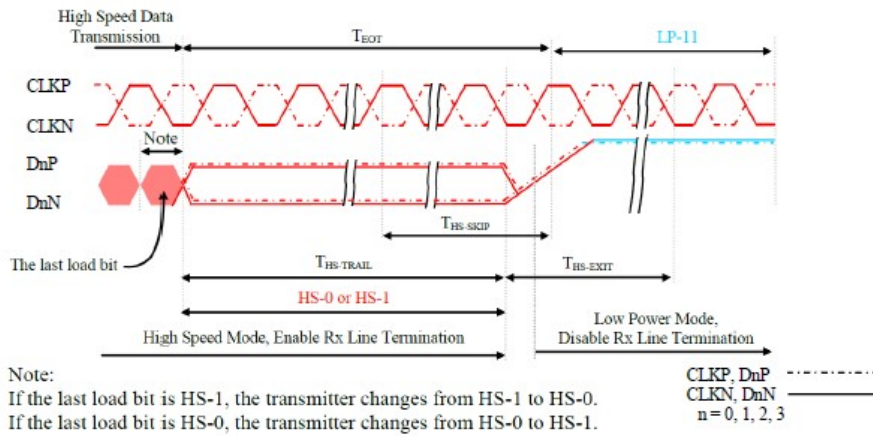


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	$55+4xUI$	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

Data Lanes from Low Power Mode to High Speed Mode

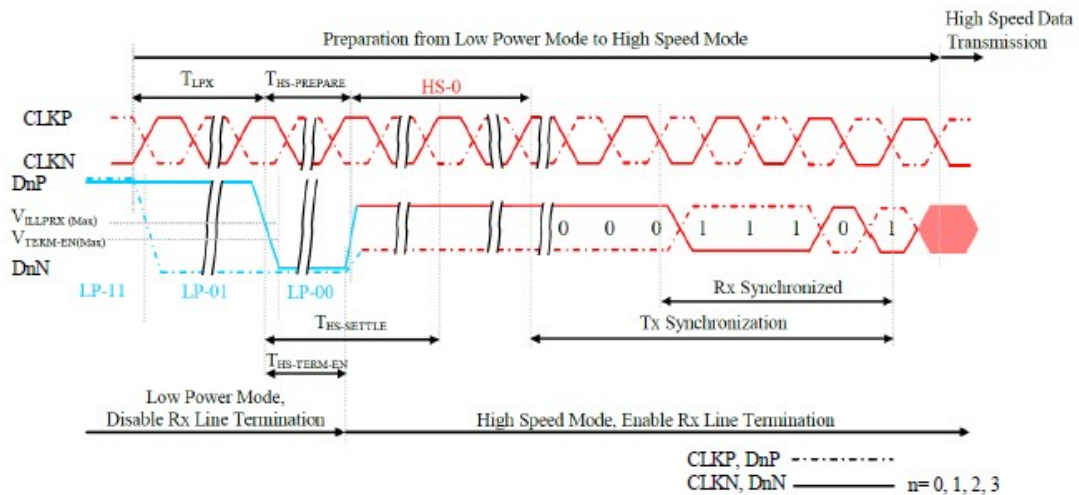


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	$40+4xUI$	$85+6xUI$	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	$35+4xUI$	ns

DSI Clock Burst – High Speed Mode to/from Low Power Mode

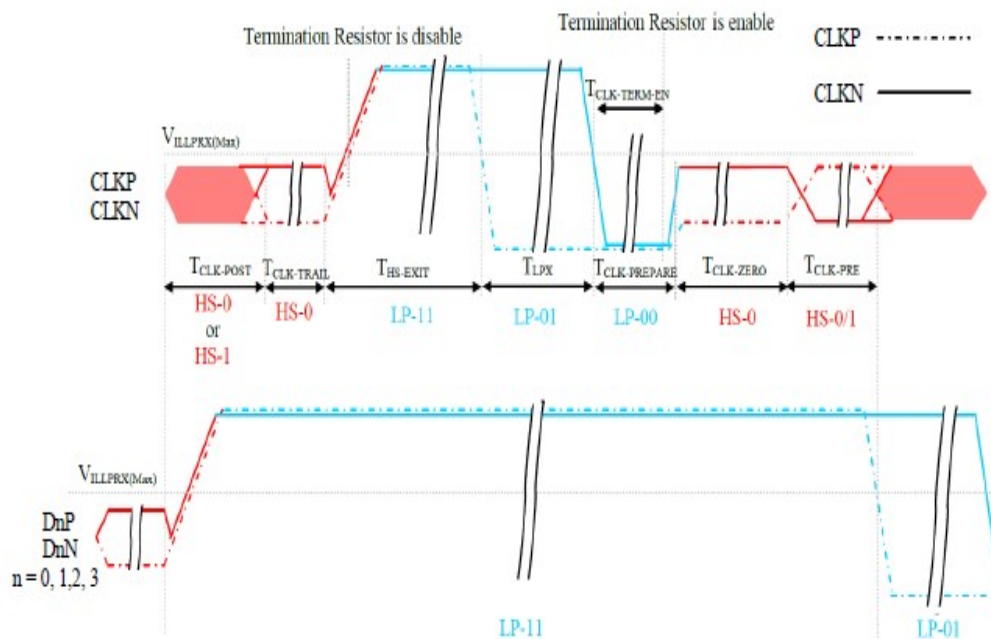
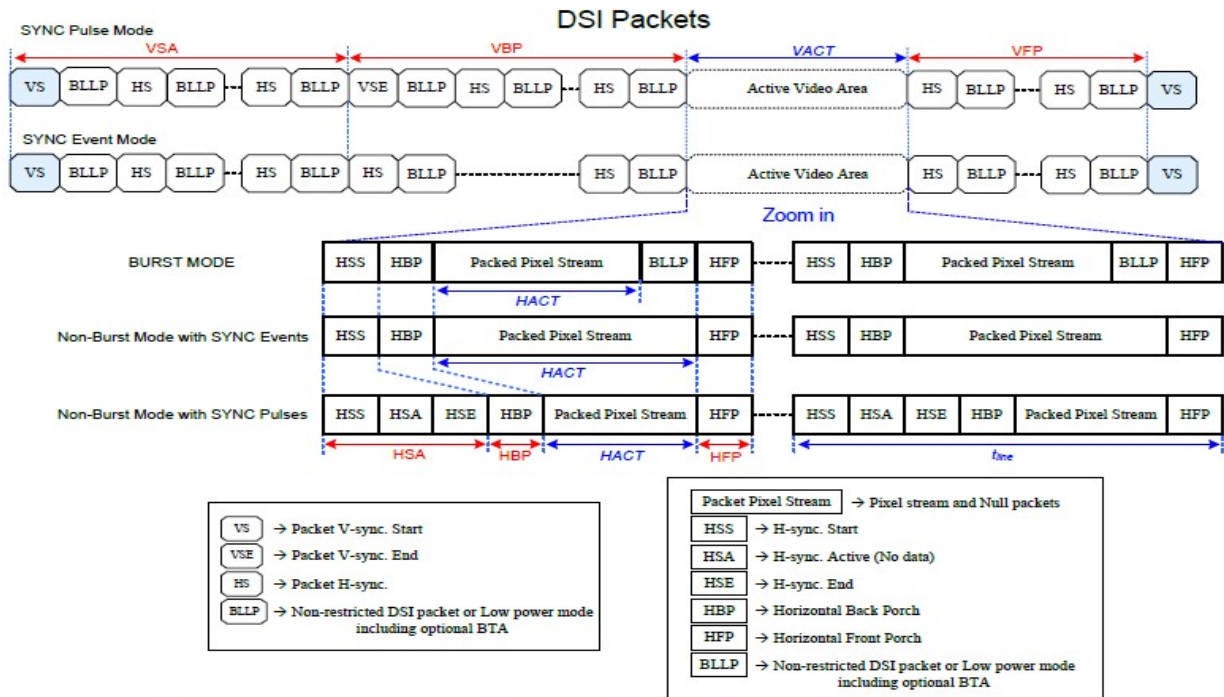


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	$60+52 \times UI$	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$8 \times UI$	-	ns

6.5 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	TBD	TBD	-	Line
Vertical Back Porch	VBP	TBD	TBD	-	Line
Vertical Front Porch	VFP	TBD	TBD	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	TBD	TBD	-	Pixel
Horizontal Back Porch	HBP	TBD	TBD	-	Pixel
Horizontal Front Porch	HFP	TBD	TBD	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	TBD		-	bps/lane
Bit rate	BR _{bps}	200		Note 5	Line

6.6 Reset Timing

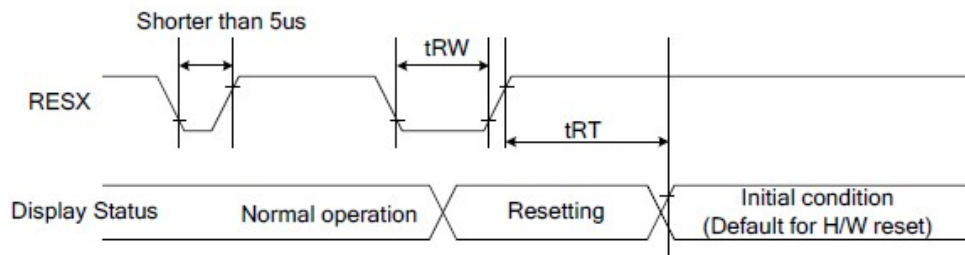


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	t_{RW}	Reset pulse duration	10		uS
	t_{RT}	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

7. Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness (with TP)	Bp	$\theta=0^\circ$ $\Phi=0^\circ$	280	350	-	Cd/m ²	1
Uniformity	Δ Bp		75	80	-	%	1,2
Viewing Angle	3:00	Cr $\geq$ 10	70	80	-	Deg	3
	6:00		70	80	-		
	9:00		70	80	-		
	12:00		70	80	-		
Contrast Ratio	Cr	$\theta=0^\circ$ $\Phi=0^\circ$	600	800	-	-	4
Response Time	T _r		-	25	35	ms	5
	T _f		-	-	-	ms	
Color of CIE Coordinate	W	x	0.263	0.313	0.363	-	1,6
		y	0.279	0.329	0.379	-	
	R	x	-	TBD	-	-	
		y	-	TBD	-	-	
	G	x	-	TBD	-	-	
		y	-	TBD	-	-	
	B	x	-	TBD	-	-	
		y	-	TBD	-	-	
NTSC Ratio	S		65	70	-	%	

Note: The parameter is slightly changed by temperature, driving voltage and materiel

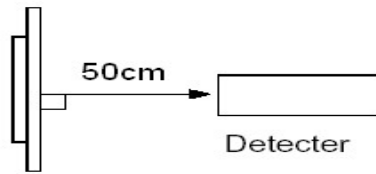
Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ8mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25 °C.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight

turning on.

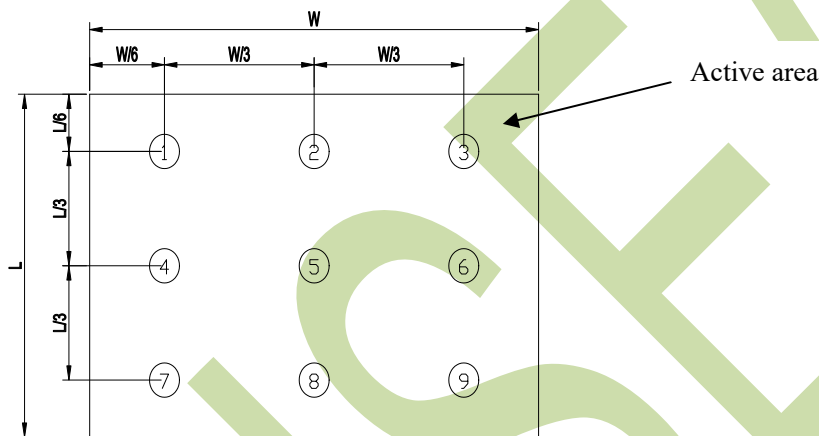


Note 2: The luminance uniformity is calculated by using following formula.

$$\Delta Bp = Bp (\text{Min.}) / Bp (\text{Max.}) \times 100 (\%)$$

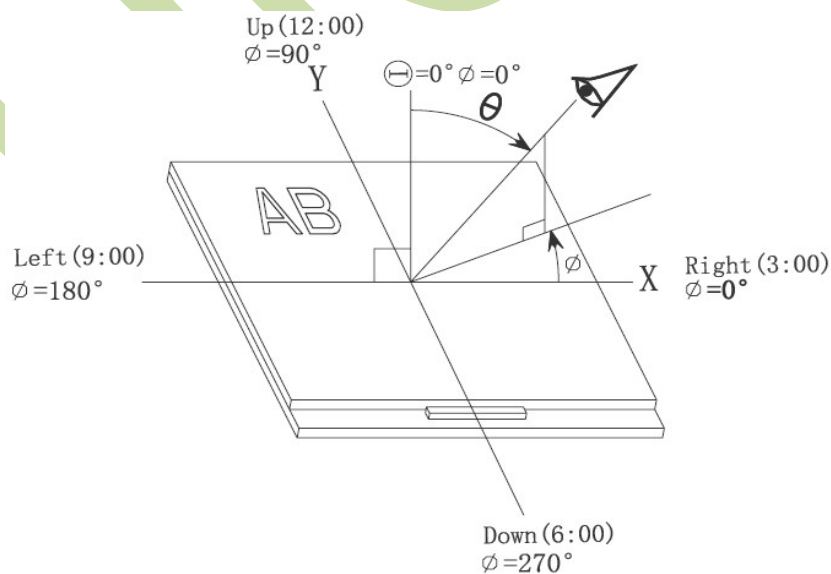
$Bp (\text{Max.})$ = Maximum brightness in 9 measured spots

$Bp (\text{Min.})$ = Minimum brightness in 9 measured spots.

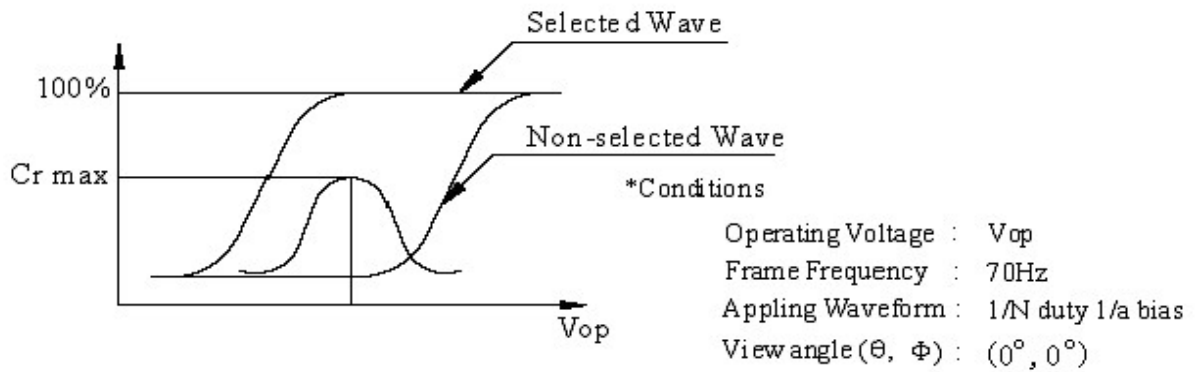


Note 3: The definition of viewing angle:

Refer to the graph below marked by θ and ϕ



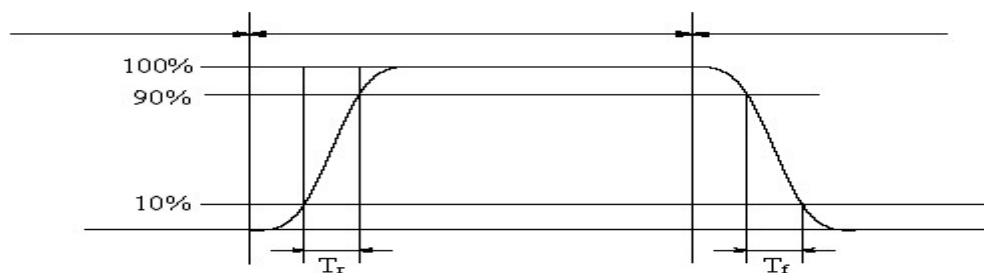
Note 4: Definition of contrast ratio.(Test LCD using DMS501)



$$\text{Contrast ratio}(Cr) = \frac{\text{Brightness of selected dots}}{\text{Brightness of non-selected dots}}$$

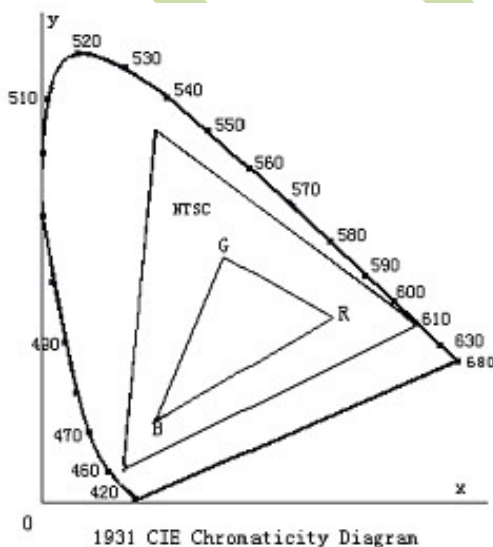
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.

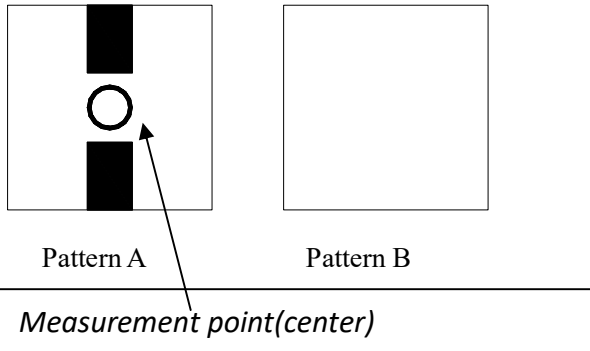


Color gamut:

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 7: Definition of cross talk.

Cross talk ratio(%)=|pattern A Brightness-pattern B Brightness|/pattern A Brightness*100



Electric volume value=3F+/-3Hex

8. Reliability Test Items and Criteria

No	Test Item	Test condition	Criterion
1	High Temperature Storage	80°C±2°C 96H Restore 2H at 25°C Power off	1. After testing, cosmetic and electrical defects should not happen. 2. Total current consumption should not be more than twice of initial value.
2	Low Temperature Storage	-30°C±2°C 96H Restore 2H at 25°C Power off	
3	High Temperature Operation	70°C±2°C 96H Restore 2H at 25°C Power on	
4	Low Temperature Operation	-20°C±2°C 96H Restore 4H at 25°C Power on	
5	High Temperature/Humidity Operation	60°C±2°C 90%RH 96H Power on	
6	Temperature Cycle	-30°C → 80°C 30min 5min 30min after 5 cycle, Restore 2H at 25°C Power off	
7	Vibration Test	10Hz~150Hz, 100m/s ² , 120min	Not allowed cosmetic and electrical defects.
8	Shock Test	Half- sine wave, 300m/s ² , 11ms	

Note: Operation: Supply 2.8V for logic system.

The inspection terms after reliability test, as below

ITEM	Inspection
Contrast	CR>50%
IDD	IDD<200%
Brightness	Brightness>60%
Color Tone	Color Tone+/-0,05

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol — Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water — Ketone — Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : $0^{\circ}\text{C} \sim 40^{\circ}\text{C}$

Relatively humidity: $\leq 80\%$

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

END